An 8-bit Digitally-controlled Low NF VGA for 5G Millimeter-wave Beamforming in 65 nm CMOS Technology

Sid Ahmed Tedjini, Sonia Salhi

Abstract—In this paper, a linear-in-dB digitally controlled variable gain low-noise amplifier (D-VGLNA) designed in 65 nm CMOS process for the 5G mm-wave phase-array subsystem is presented. Based on the current steering technique, the designed 8-bit D-VGLNA achieves a gain range of 22 dB from -12 dB to +10 dB while it consumes 9.6 mW (without buffers). By boosting up the input transconductance thanks to a cross-coupled technique, the designed D-VGLNA achieves a noise figure of 2.3 dB, and 7 dB at maximum and 0 dB gain, respectively. It shows an input-output phase shift insensitivity to gain setting thanks to parasitic capacitance mitigation by holding the parasitic capacitance at common junction cascode transistor constant during gain setting. The DVGLNA returns a maximum of -6.5 dBm of 1dB compression point.

***Keywords*—VGA, LNA, 5G, phase array, beamforming.**

I. Introduction

The last couple of decades have been witnessing a major development in CMOS technology making a drastic increase in the transition frequency of MOS transistors. This development in lithography opened up the opportunity for integrated circuit design for frequency bands beyond 20 GHz where large bandwidth and low latencies applications became possible in contrast with the crowded sub-6 GHz band where the majority of communication standards lie [1–3]. In that context, the fifth-generation standard of mobile communication has the aim of providing gigabit-per-second range connectivity necessitating Giga-Hertz range bandwidth. The 28 GHz band has been identified as one possible band for 5G communication [4]. In that context, the effort has been made for developing 5G IC receivers [5, 6]. Designing transceivers for such applications is not an easy task since the incoming radio frequency signal suffers from a strong loss due to the propagation in the atmosphere as well as surrounding obstacles [7, 8]. Increasing the transmitter power is not a possible solution since it increases the power dissipation of the power amplifier particularly if it is integrated in silicon technology. Increasing the antenna gain at the receiver side is then the possible solution to compensate for the propagation loss. However, because of the antenna's narrow beam, signal reception becomes impossible in the case where the transmitter and receiver are not in-sight. The solution comes from receivers based on the phase array system, also called beamformers, where a highly effective antenna gain is achieved thanks to a network of omnidirectional antennas [7] as depicted in Fig. 1. In a phase array system, each antenna sens the incoming radio frequency signal with a given delay with respect to other antennas. In order to avoid a signal-destructive combination prior to frequency down-conversion, each channel incorporates a phase shifter that introduces a given loss.

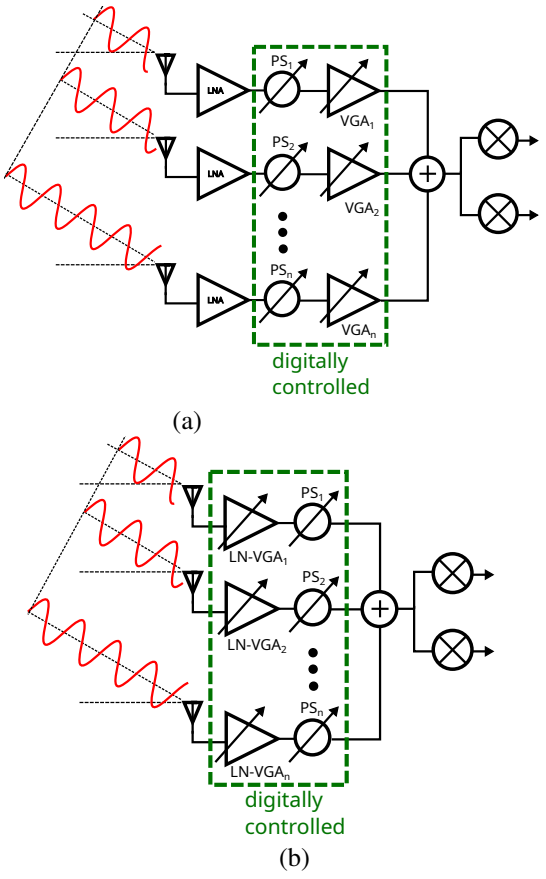

Fig. 1: phase array system (a) conventional architecture, (b) merged VGA, LNA architecture

As depicted in Fig. 1, beamformer receivers integrate a variable gain amplifier to compensate for the loss of the phase shifter [9]. The VGA has to maintain input and output return loss as well as

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phase variation constants during gain sitting, which may result in undesired additional phase and gain variations.

As depicted in Fig. 1(a), the traditional channel path consists of cascading low noise amplifier, phase shifter, and variable gain amplifier. Having a performant VGA in terms of noise can lead to a merged architecture where the LNA and the VGA are merged as a single bloc resulting in complexity reduction as well as power dissipation reduction as illustrated in Fig. 1 (b).

Many analog and digital gain control techniques have been reported in past years. Most popular techniques are current steering [10], variable g_m [11], reflection-type attenuator [12], or ladder-type attenuator VGA [13].

The current steering technique is suitable for mm-wave because of the simplicity of its implementation and also low power dissipation requirement.

In this paper, a digitally controlled 8-bit variable low-noise amplifier is presented. Section II. starts by describing the base of the D-VGLNA which consists of a cross-coupled cascade amplifier. The principle of gain control with current steering is presented in section III. along with a description of the designed D-VGLNA. Simulation results are presented in section IV. before the conclude this paper in section V..

II. MM-WAVE LOW-NOISE AMPLIFIER

A. Technology

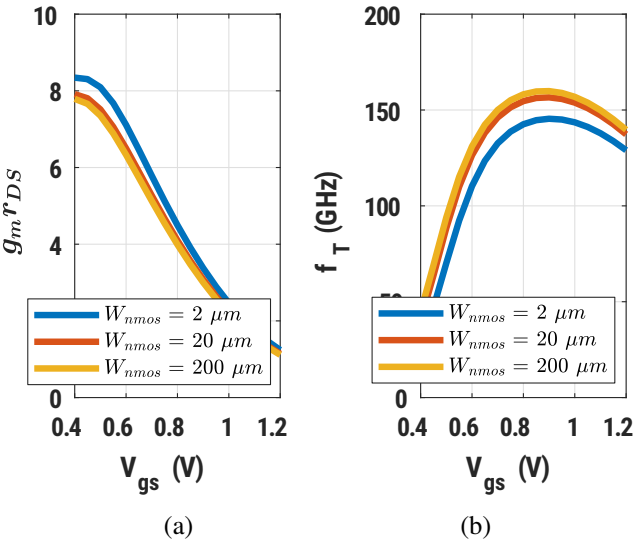
The design of an amplifier at millimeter-wave frequencies requires a large gain-bandwidth product, denoted GBW. The GBW depends on the transistor self-gain as well as its frequency transition denoted f_T. The MOS self-gain, denoted SG, is defined as $g_m \times r_{ds}$, where g_m, and r_{ds} stand for the MOS transconductance and its output resistance, respectively. While frequency transition of the MOS transistor is defined as the frequency of the unity gain's current and is given by the equation 1 which suggests that it is proportional to the transistor g_m.

$$f_T = \frac{g_m}{2\pi(C_{\text{GS}} + C_{\text{GD}})} \tag{1}$$

Fig 2(a) shows the MOS SG variation as a function of V_{GS} for a 65 nm NMOS transistor. The maximum SG is achieved when the MOS transistor operates on a weak inversion region, meaning when V_{GS} is inferior to the threshold voltage. On the other hand, as Fig. 2(b) illustrates, MOS f_T variation according to equation 1 as a function of gate-to-source voltage (V_{GS}) for different gate width, shows that the highest f_T value is achieved when the transistor is operating in strong inversion, meaning for V_{GS} much higher than the threshold voltage V_{TH}. For 65 nm standard CMOS technology, the NMOS device reaches a maximum f_T of 160 GHz.

B. Cross-coupled Cascode Amplifier

As demonstrated in the previous section, transistors are biased on strong inversion in order to achieve the highest f_T. To overcome the insufficient gain resulting from a weak transistor's self-gain in strong inversion operation, the amplifier gain can be raised by cascading a second NMOS device and boosting up the input



(a) (b)

Fig. 2: (a) MOS self-gain variation as function of V_{GS}, (b) NMOS f_T variation as function of V_{GS}

gm thanks to the cross-coupling technique as illustrated in Fig. 3. The input effective transconductance, denoted $g_{\text{m1,eff}}$ is given by [14]:

$$g_{\text{m1,eff}} = \left(1 + \frac{C_c}{C_c + C_{\text{GS}}}\right) g_{\text{m1}}, \tag{2}$$

where C_{GS} is the gate-to-source capacitance of transistors $M_{1,2}$. The boosting amplification factor, denoted A is equal to $C_c/(C_c + C_{\text{GS}})$. If C_c is chosen large enough in comparison with C_{GS}, then $g_{\text{m1,eff}} \approx 2g_{m1}$.

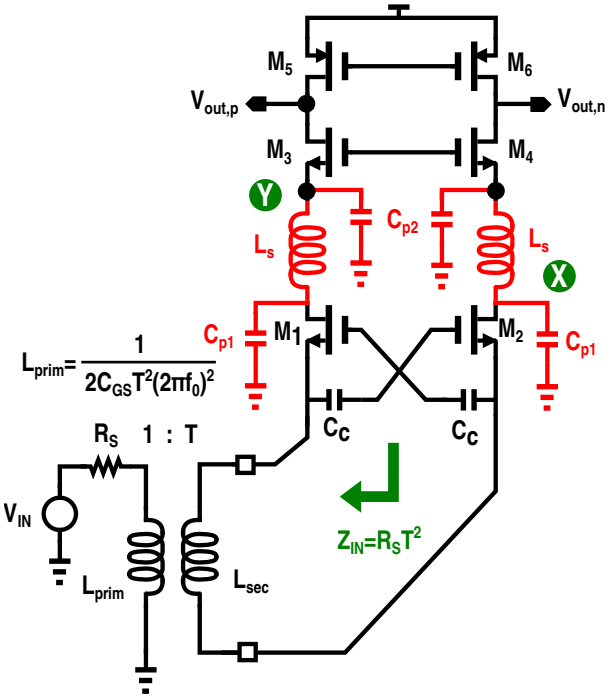


Fig. 3: Cross-coupled cascode amplifier with series shunt peaking inductor

The input transformer brings a couple of advantages. Firstly, it provides single-to-differential transformation creating the input

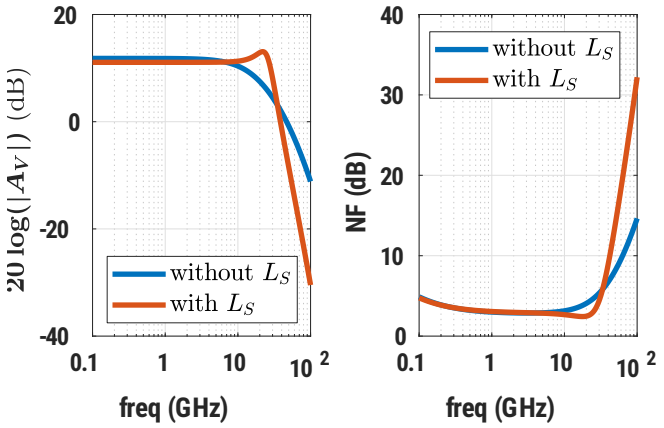


Fig. 4: voltage gain and NF as function of RF frequency of Cascode amplifier with and without series inductive peaking technique

differential signals needed to implement the cross-coupled technique. Secondly, the secondary-to-primary turn ratio increases $M_{1,2}$ noise circulation which helps to decrease the noise factor as shown in section C.. The transformer secondary inductor is chosen to resonate out $2C_{\text{GS1}}$. Hence, L_{prim} is given by:

$$L_{\text{prim}} = \frac{1}{2C_{\text{GS}}T_{\text{in}}^2(2\pi f_0)^2} \tag{3}$$

where T_{in} is transformer turn ratio, and f_0 frequency of incoming RF signal.

The voltage gain of the circuit depicted in Fig. 3 at low frequencies is given by:

$$|A_v| = g_{\text{m1,eff}} \times \left[r_{\text{o3}} + r_{\text{o1}}(1 + g_{\text{m3}}r_{\text{o3}})\right] \parallel r_{\text{o5}} \tag{4}$$

Fig. 4(a) shows the gain as well as the NF of the circuit of Fig. 3. Although C_{GS1} is resonated out by the secondary inductor, the gain starts to roll off beyond 10 GHz due to the parasitic capacitance, loading node X. In addition, C_X ($C_{\text{p1}} + C_{\text{p2}}$) may also increase noise.

Furthermore, as the impedance loading the input device is seen by the input port, the parasitic capacitance $C_X = C_{\text{p1}} + C_{\text{p2}}$ is also affecting input impedance, where C_{p1} and C_{p2} depend on the $M_{1,2}$ and $M_{3,4}$ intrinsic capacitances.

To overcome the drops of the A_V a decoupling of C_{p1} and C_{p2} is necessary thanks to series inductive peaking as shown in Fig. 3.

In fact, the impedance seen at the input RF port is given by:

$$Z_{\text{in}}(s) = \frac{1}{T_{\text{in}}^2}\left(\frac{Z_X(s) + r_{\text{o1}}}{1 + g_{\text{m1}}(1 + A)r_{\text{o1}}}\right) \tag{5}$$

where r_{o1} denotes the $M_{1,2}$ output resistance, and $Z_X(s)$ is the impedance looking back at node X as depicted in Fig. 3. Assuming the $1/g_{\text{m3}}$ the resistance looking back at M_3 source, $Z_X(s)$ is given by equation 6 where s is the Laplace variable.

$$Z_X(s) \approx \frac{1 + sg_{gm3}L_S + s^2L_sC_{\text{p2}}}{g_{m3} + s(C_{\text{p1}} + C_{\text{p2}}) + s^2g_{m3}L_sC_{\text{p2}} + s^3C_{\text{p1}}C_{\text{p2}}L_s} \tag{6}$$

The parasitic capacitor C_{p1} can be approximated by Miller theorem as $C_{\text{gd1}}(1 + g_{\text{m1}}(1 + A)(r_{\text{o1}} \parallel 1/g_{\text{m3}}))$, while the C_{p2} is equal to C_{gs3}. Assuming the inductor is chosen to resonate out C_{p2}, if one makes $C_{p2} = C_{p2}$ the $Z_X(s)$ becomes a purely real function, and is expressed as follows:

$$Z(s) = \frac{g_{\text{m3}}L_S}{C_{\text{p2}}} \tag{7}$$

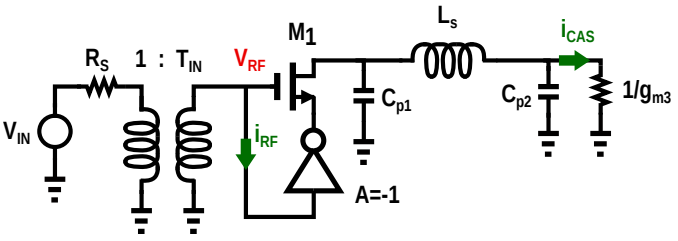


Fig. 5: Half-circuit input impedance analysis

As a consequence, the input impedance seen at the input port is:

$$Z_{\text{in}} = \frac{g_{\text{m3}}L_S + C_{\text{p2}}r_{\text{o1}}}{T_{\text{in}}^2(1 + g_{\text{m1}}(1 + A)r_{o1})} \tag{8}$$

considering the decoupling inductor L_S at the source cascode device, the input and output current ratio as depicted in Fig. 5 is given by:

$$\frac{i_{\text{cas}}}{2g_{\text{m1}}V_{\text{RF}}} \approx \frac{g_{\text{m3}}}{g_{\text{m3}} + s(C_{p1} + C_{p2}) + s^2L_sC_{p1}g_{\text{m3}} + s^3L_sC_{p1}C_{p2}} \tag{9}$$

Consistently, Fig. 6 shows the simulation of $i_{\text{cas}}/2g_{\text{m1}}V_{\text{RF}}$ versus RF frequency demonstrates the low-pass profile of the current gain with a resonance at 28 GHz thanks to a proper L_s value.

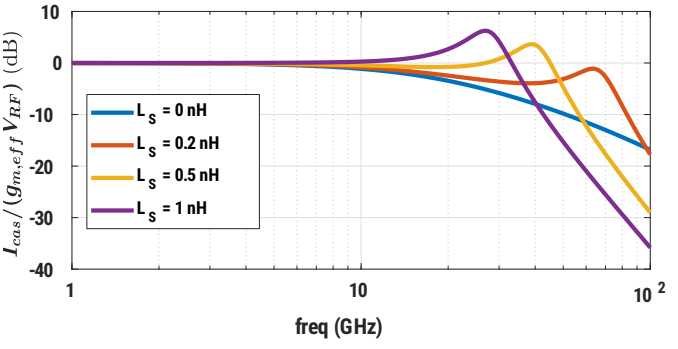


Fig. 6: Schematic-level simulation of $i_{\text{cas}}/2g_{\text{m1}}V_{\text{RF}}$ versus RF frequency

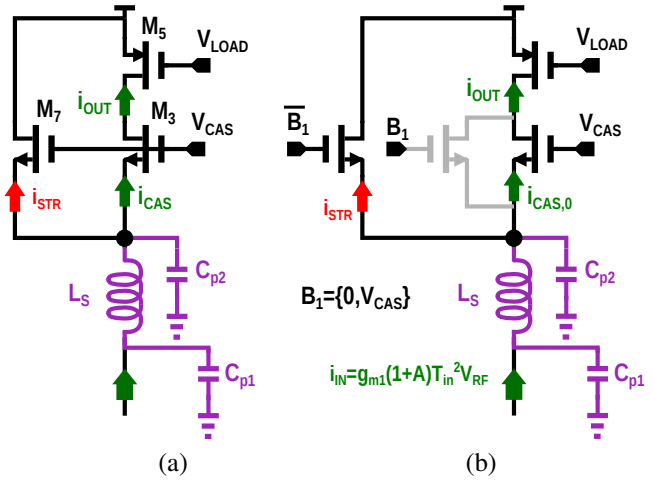


Fig. 7: (a) 1-bit half circuit VGA, (b) C_{p2} variation mitigation for 1-bit VGA

C. *Noise analysis*

As the $1/g_{\text{m3}} << r_{\text{o1}}$ the noise contribution of cascade device is negligible. Assuming that input transistors are the main noise source of the cascode amplifier depicted in Fig. 3. The noise factor is given by :

$$F \approx 1 + \frac{\gamma}{T_{\text{in}}^2 R_S g_{\text{m1}}(1+A)^2} \tag{10}$$

where γ is the noise excess factor of the MOS device and is in order of 3 for 65 nm CMOS technology.

If the denominator of the second term of the right side of the equation. 10 is equal to unity, the amplifier achieves an excessive noise figure 6 dB, according to the above equation. The noise figure can be drastically reduced if $T_{\text{in}}^2 R_S g_{\text{m1}}(1+A)^2 << 1$ while the amplifier is kept matched to RF port impedance. Assuming $A = 1$, and substituting R_S by R_{IN} as given in equation 8, the expression of F under matching condition is re-written as:

$$F \approx 1 + \frac{\gamma r_{\text{o1}}}{(1+A)(g_{\text{m3}} L_S + C_{\text{p2}} r_{\text{o1}})} \tag{11}$$

Thus, the topology of Fig. 3 allows to match the input impdende to R_S which less to 3 dB NF since $r_{\text{o1}}/(2(g_{\text{m3}} L_S + C_{\text{p2}} r_{\text{o1}}) << 1$.

III. D-VGLNA AMPLIFIER

A. *VGA Gain setting principle*

Fig. 7(a) shows the half-side of Fig. 3 including a current steering device also called current bleeding [15]. Obviously, the output current drops because of the current steering, and consequently the amplifier output voltage drops as well.

As the g_{m7} increases, the current quantity steered increases which decreases the amplifier gain. However, C_{p2} is gain-dependent since $C_{\text{P2}} = C_{\text{GS7}} + C_{\text{GS3}}$. To tackle this issue, the cascode device is settled digitally too.

The output current is now given by:

$$i_{\text{out}} = i_{\text{in}} \left[1 - g_{m7} \left(\frac{r_{o7}}{1 + g_{m7} r_{o7}} \parallel \frac{r_{o3} + r_{o5}}{1 + g_{m3} r_{o3}} \right) \right] \tag{12}$$

Assuming $1/g_{m3} << r_{o3}$, and $1/g_{m7} << r_{o7}$, the following approximation can be done.

$$i_{\text{out}} \approx i_{\text{in}} \left[1 - g_{m7} \left(\frac{1}{g_{m7}} \parallel \frac{1}{g_{m3}} \right) \right] \tag{13}$$

The current gain defined as $A_i = i_{\text{cas}}/i_{\text{in}}$ is given by:

$$A_i \approx \frac{g_{m3}}{g_{m3} + g_{m7}} \tag{14}$$

Consequently, the voltage gain A_V can be expressed as a function of A_i, and losses due to steering transconductance, and is given by:

$$A_V \approx r_{\text{out}} g_{\text{m1}} (1+A) T_{\text{in}}^2 \frac{g_{m3}}{g_{m3} + g_{m7}}. \tag{15}$$

The expression of current gain suggests that if cascode and bleeding devices as sized identically in such a way to have $g_{m3} = g_{m7}$ ($W_3 = W_7$), the voltage gain drops with 6 dB as well the current gain. For 3 dB drop, $A_i = 1/\sqrt{2}$, it follows that $g_{m7} = (\sqrt{2} - 1) g_{m3}$.

Therefore, the gain can be settled by making g_{m7} variable. In order to set the gain digitally in the context of a beamformer receiver, the steering device is substituted by a series of transistors settled digitally.

Although the MOS is switched OFF, its parasitic gate-to-source capacitance still exists because of overlapping capacitance. Therefore, because $C_{\text{P2}} = C_{\text{GS3}} + C_{\text{GS7}}$, the $Z_X(s)$ becomes gain dependent and thus the input impedance which is a drawback for other channel paths. To tackle this issue, a simple solution is to switch off a replica transistor, placed in parallel with cascode device, while the steering device is switched on, as shown in Fig. 7(b). In this 1-bit steering-vga scenario, the C_{p2} expression is given by:

$$C_{\text{p2}} = \frac{2 C_{\text{OX}} L}{3} (W_{\text{STR,ON}} + W_{\text{CAS}}) + C_{\text{OV}} W_{\text{STR,OFF}} \tag{16}$$

Because the replica device has the same channel width as the steering device, when the B_1 signal drops to zero, C_{p2} stays unchanged.

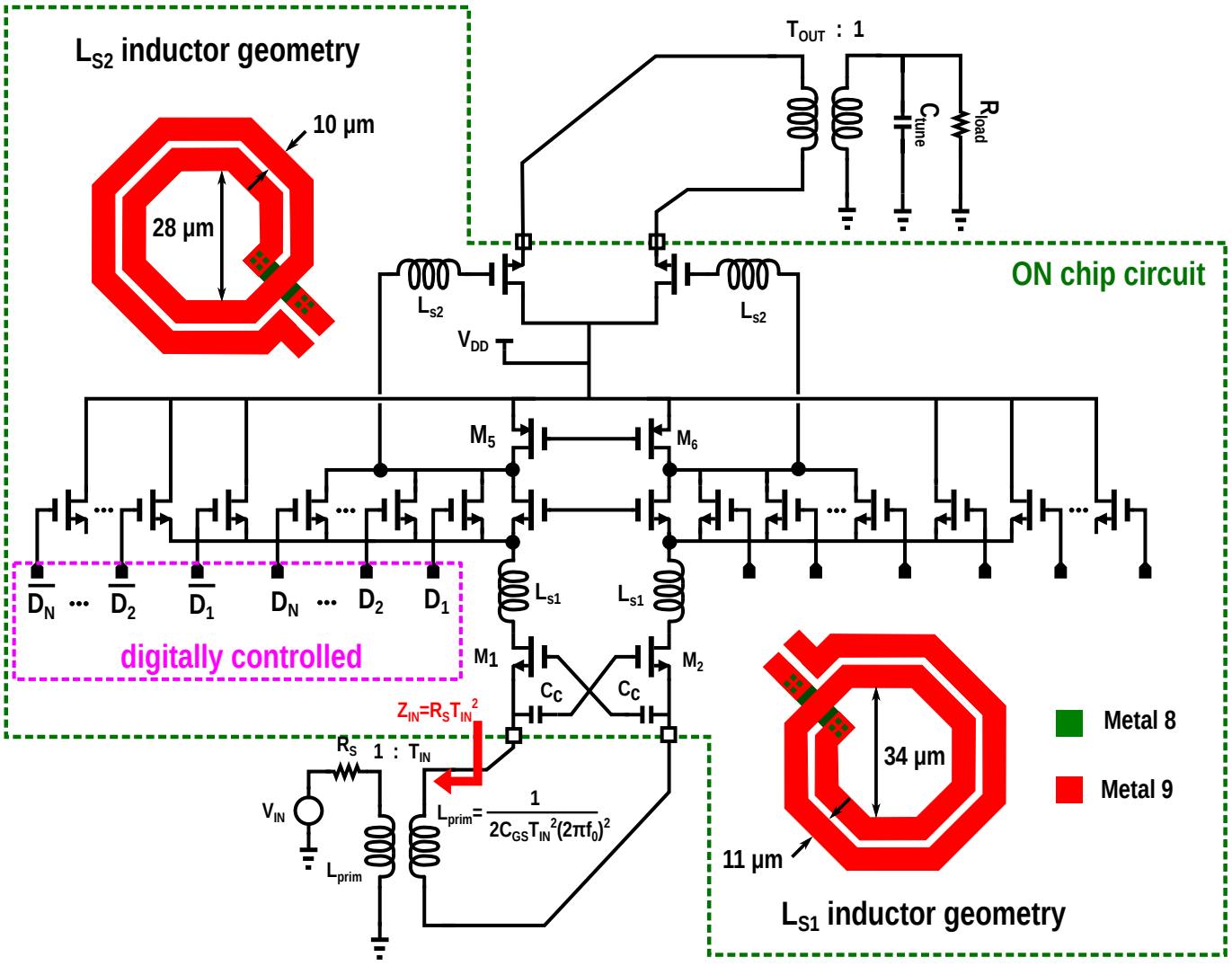


Fig. 8: 8-bit digitally-controlled variable-gain Low-noise amplifier (D-VGLNA)

B. 8-bit digitally-controlled VGA implementation

The implementation of the 8-bit digitally controlled VGA based on the principle described in section A. is depicted in Fig. 8.

An off-chip high-quality factor transformer with a turn ratio of $\sqrt{2}$ is used which is not affecting the noise performance of the VGA. The input transconductance devices $M_{1,2}$ sees an input impedance of 100 Ω which will improve noise circulation and reduce the $M_{1,2}$ channel noise accounted for in the noise factor. The coupling capacitor C_C is much larger than C_{GS} leading to a boosting factor of one. As depicted in Fig. 8, the decoupling inductor L_{S1} is 2 turns coil with width and radius of 11 μm and 34 μm respectively, achieving an inductor value of 985 pH with a quality factor of 7 at 28 GHz. The cascode device is implemented thanks to a series of parallel NMOS transistors, controlled digitally with an 8-bit binary word $\{D_1, D_2, ..., D_8\}$, where the high level D_i is about 0.8 V in order to maintain the cascode devices into saturation when they are switched on. The steering operation is guaranteed by a series of parallel NMOS devices of the same size as cascode devices. controlled with $\{\overline{D_1}, \overline{D_2}, ..., \overline{D_8}\}$ in such way to keep the C_{P2} constant. The C_{P2} expression of 16 is re-written as:

$$C_{p2} = \frac{2C_{OX}L}{3}W_{CAS,0} + \sum_{i=1}^{k}\left(\frac{2C_{OX}L}{3}W_{CAS,i} + C_{OV}W_{STR,i}\right) + \sum_{i=k+1}^{N}\left(\frac{2C_{OX}L}{3}W_{CAS,i} + C_{OV}W_{STR,i}\right) \quad (17)$$

Where the first term stands for the gate-to-source capacitance of the non-controlled cascode devices that stay on for all gain setting configurations, and guarantee the minimum gain. The second term accounts for the gate-to-source capacitance of all steering devices that are set on saturation of a given gain setting plus the gate-to-source capacitance for all replica devices (parallel to cascode) that are on the cutoff region. Similarly the third term accounts for the gate-to-source capacitance of cutoff-biased cascode and steering devices.

The outlined $g_{m3} - g_{m7}$ relationship can be generalized to derive a digitally-controled VGA $g_{m3} - g_{m7}$ relationship of equation for -3n dB of gain drop.

$$\sum_{i=1}^{k} g_{m,str,i} = (2^{n/2} - 1)\left(g_{m,cas,0} + \sum_{i=k+1}^{N} g_{m,cas,i}\right) \quad (18)$$

The above equation suggests that the voltage gain can be decreased by an attenuation factor, denoted AF_{dB}, of 3n dB by switching ON parallel steering devices digitally, where $n = 1, 2, 3...$ On linear domaine, $AF = \sqrt{2}, 2, 2\sqrt{2}, 4,$ etc. Maximum gain is obtained when all steering transistors are switched OFF. The differential output is connected to differential source followers through a 2 turns coil decoupling inductors (L_{s2}) with width and radius of 10 μm and 28.5 μm respectively, achieving an inductor value of 708 pH with a quality factor of 10.5 at 28 GHz. An output balun transformation is achieved by an off-chip one-turn ratio transformer that matches the VGA output impedance to 50 Ω. The capacitor C_{tune} is used to resonate out the secondary at 28 GHz. Fig. 9. shows the plot of A_i as a function of RF frequency for different VGA configurations. When all cascaded transistors are switched ON, $A_i \approx 1$

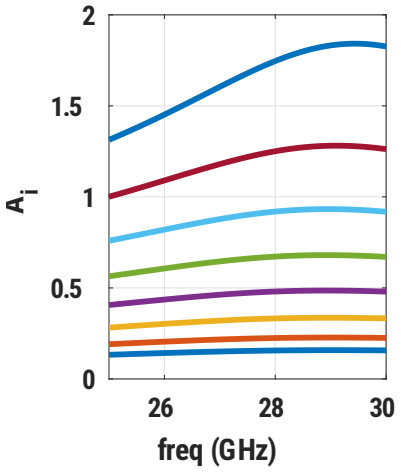


Fig. 9: Current gain for different V_{GS} configuration

As cascode devices start to be switched OFF, the current gain drops to 0.75, etc.

C. Noise analysis

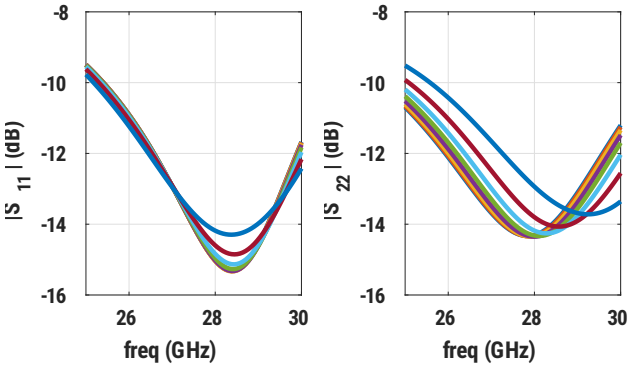
When the noise contribution from the steering devices and the load transistors is taken into account, the noise factor is expressed by 19. The second term of the noise factor represents the noise contribution from the input transistors $M_{1,2}$, while the third and the fourth terms represent the loads, and the steering devices, respectively. The noise accounted for from the input gm and the loads are multiplied by a multiplication factor (between brackets in equation 19) which catches the gain setting effect. In fact, at the maximum gain setting, the index $k = 0$, therefore, the multiplication factor is reduced to unity. However, for the minimum gain setting when $k = N$, the multiplication factor reaches its maximum value of $1 + \sum_{i=1}^{N} g_{\text{m,str,i}}/g_{\text{m,cas,0}}$, increasing drastically the noise contribution of $M_{1,2}$ as well as $M_{5,6}$ transistors.

IV. Simulation Results

All performances presented in this section are obtained by simulation with the Cadence Spectre tool.

A. VGA performance

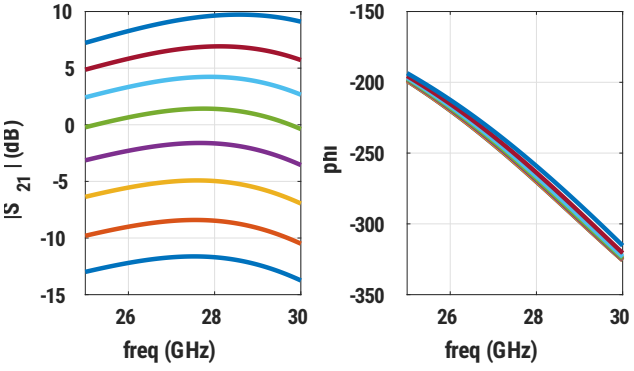
Fig. 10(a) shows the input return loss as a function of the frequency for different configurations. Clearly, the S_{11} experiences only a little variation over all frequencies with a maximum value of -14 dB in the vicinity of 28 GHz. The same observation is made for the output return loss shown in Fig. 10 which is less than -13 dB around 28 GHz thanks to the use of source followers. Fig. 11(a) shows the variation of S_{21} as a function of frequency for all VGA configurations.



(a) (b)

Fig. 10: (a) D-VGLNA Input return loss, (b) D-VGLNA output return loss

At 28 GHz, the S_{21} is equal to 10 dB when all steering devices are OFF as mentioned in section B., and drops with a pace of 3dB as the steering is switched ON to fall to -12 dB when all steering devices are ON. Simulation of phase shift from input to output is shown in Fig. 11(b). As the devices are switched ON and OFF, the phase shift does not vary much.



(a) (b)

Fig. 11: (a) D-VGLNA power gain magnitude, (b) D-VGLNA power gain phase

Noise figure reach a minimum value of 2.3 dB at 28 GHz when the power gain is maximum and a value of 7 dB when the power gain is equal to 0 dB.

Fig. 13 shows the variation of -1 dB compression point for different D-VGLNA gain settings including the output buffers simulated with harmonic balance. The simulation returns a 1dB CP between -5 and -6.5 dB.

$$F = 1+\left(1+\frac{\sum_{i=1}^{k} g_{\mathrm{m,str,i}}}{g_{\mathrm{m,cas,0}}+\sum_{i=k+1}^{N} g_{\mathrm{m,cas,i}}}\right)\left[\frac{\gamma}{R_S g_{\mathrm{m1}}(1+A)^2 T_{\mathrm{IN}}^2}+\frac{(1+g_{\mathrm{m1}}R_s(1+A)T_{\mathrm{IN}}^2)^2}{R_s g_{\mathrm{m1}}^2 r_{\mathrm{o5}}(1+A)^2 T_{\mathrm{IN}}^2}\right]+\frac{g_{\mathrm{m7}}\gamma}{R_S g_{\mathrm{m1}}^2 T_{\mathrm{IN}}^2}\left(\frac{1+g_{\mathrm{m1}}R_S(1+A)T_{\mathrm{IN}}^2}{1+A}\right)^2 \tag{19}$$

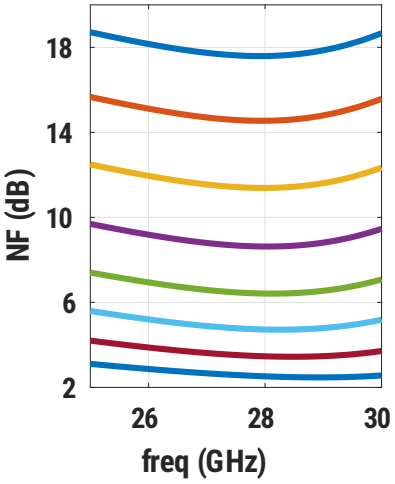


Fig. 12: D-VGLNA noise figure

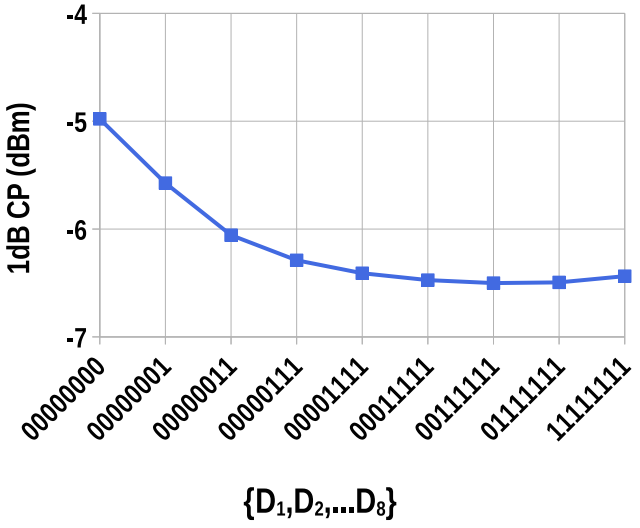


Fig. 13: 1 dB compression point

B. Layout implementation, hunts, and recommendations

Although post-layout simulation was not included, the presented figures of merit can still be achieved when the circuit is implemented in standard CMOS technology. Careful layout design is crucial to minimize additional parasitic capacitances at critical nodes and input parasitic resistance, as they can significantly degrade gain and noise figure at 28 GHz. In this context, the following suggestions and recommendations may be helpful for layout implementation while operating at 28 GHz.

- **The distance between the input signal pads and transistors M_1 and M_2 should be kept as short as possible. It is also highly recommended to use the top thick metal for the signal path to minimize input resistance, which could lead to NF degradation.**
- **Parasitic capacitances resulting from metal interconnections have to be accounted for in C_{p1} and C_{p2} estimation. This can be done effectively by extracting parasitic components with a dedicated tool after the layout has been completed. Thus, inductor geometry has to be adjusted accordingly to prevent any deviation in voltage gain from the desired value.**
- **Matching techniques, such as common centroid, are highly recommended for layout design of differential pair implementation, especially in current steering devices, due to the silicon's local gradient.**

  As mentioned in section III. A. maintaining a constant $Z_{\mathrm{in}}(s)$ and thereby stabilizing C_{p2} when the steering devices are activated and deactivated is essential for VGA operation. For instance, when the $M_{\mathrm{STR,i}}$ layout does not match its replica device, capacitance at node Y varies with changes in the polarity of D_{i}, as suggested by equation 17 . As a consequence, $Z_{\mathrm{in}}(s)$ deviates from the matching condition, resulting in the input return loss straying from its optimal value for different configurations of D_{i}. This leads to a spread of S_{11} in the vicinity of 28 GHz, rather than producing close curves as illustrated in Fig. 10.

V. Conclusion

In this paper, a low-noise variable gain amplifier is designed using a 65 nm CMOS standard process for a 28 GHz beam steering receiver. The VGA gain is set using digitally controlled current steering devices. The parasitic capacitances at the critical node are mitigated thanks to a set of digitally controlled replica devices, resulting in phase variation, input and output return loss insensitivity to gain setting, which can be performed in the digital domain. Thanks to this simple technique, the constant input and output return loss and the sub-3 dB NF demonstrate the VGA's capability to operate as an LNA, consequently reducing circuit complexity, cost, and power consumption for the overall beamformer receiver in the context of 5G mm-wave.

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