Advanced Control of Shunt Active Power Filter based on Flying Capacitor Multicellular Inverter using Backstepping and PS-PWM

Kheira Hemici and Mohand Oulhadj Mahmoudi

Abstract−This paper presents an advanced nonlinear control strategy for a Shunt Active Power Filter (SAPF) utilizing a Flying Capacitor Multicellular Inverter (FCMLI) to improve power quality in electrical distribution systems. The proposed control is based on the Backstepping technique, known for its ability to handle nonlinear system dynamics and guarantee global stability. To ensure efficient inverter operation and capacitor voltage balancing, Phase-Shifted Pulse Width Modulation (PS-PWM) is employed. The effectiveness of the proposed Backstepping controller is evaluated against a traditional Proportional-Integral (PI) controller. Simulation results demonstrate that the proposed method outperforms the conventional PI controller in terms of total harmonic distortion (THD), transient response, and capacitor voltage balance.

***Keywords*−Shunt active power filter, flying capacitor multicellular inverter, backstepping control, harmonic mitigation.**

NOMENCLATURE

SAPF	Shunt Active Power Filter
FCMLI	Flying Capacitor Multicellular Inverter
PS-PWM	Phase-Shifted Pulse Width Modulation
PI	Proportional-Integral
BC	Backstepping Controller
THD	Total Harmonic Distortion
RMS	Root Mean Square
PCC	Point of Common Coupling
SRF	Synchronous Reference Frame

I. INTRODUCTION

Power quality has become a major concern due to the proliferation of nonlinear loads in modern electrical grids. Shunt Active Power Filters (SAPFs) are widely employed to compensate for current harmonics and reactive power [1]- [3]. The integration of multilevel inverters, particularly Flying Capacitor Multicellular Inverters (FCMLIs), into SAPFs provides additional benefits such as reduced switching losses, improved voltage quality and modularity. Numerous researchers have explored and tested a variety of control methodologies tailored to FCMLI-based SAPFs [4]-[11]. These strategies aim to enhance the dynamic performance, efficiency, and reliability of the system while ensuring compliance with stringent power quality standards.

Manuscript received September 17, 2025; revised November 2, 2025.

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Digital Object Identifier (DOI): 10.53907/enpesj.v5i2.338

The multilevel structure of FCMLIs provides significant advantages, such as reduced harmonic distortion, improved voltage waveforms, and greater flexibility in voltage control. However, FCMIs introduce complexities in control due to the floating nature of their capacitors and the need for voltage balancing [12]-[14]. Traditional control strategies like PI controllers often fail to maintain performance under varying load conditions or dynamic disturbances. To address these limitations, this study proposes a nonlinear Backstepping control scheme integrated with PS-PWM, providing improved harmonic mitigation and capacitor voltage regulation.

Backstepping is a powerful recursive design methodology that systematically builds a robust nonlinear control law, guaranteeing global asymptotic stability for systems in strict feedback form [15]-[17]. This method is especially well-suited for complex power electronic converters because it explicitly accounts for the system's nonlinearities. Consequently, it delivers superior dynamic performance, disturbance rejection, and accurate tracking compared to conventional linear control approaches.

Our numerical simulations clearly demonstrate the effectiveness of this proposed backstepping-based control strategy in achieving the outlined control goals, ensuring stable operation, optimal performance, precise flying capacitor voltage balancing, and effective harmonic current compensation. This paper is organized as follows: Section II details the mathematical model of the SAPF-FCMLI in the d-q reference frame; Section III discusses the proposed backstepping controller synthesis; Section IV presents the simulation results and their interpretation; Section V concludes the paper II

II. MATHEMATICAL MODEL OF THE SAPF-FCMLI IN THE D-Q REFERENCE FRAME

In this section, the topology of the three-phase SAPF FCMLI is presented, along with its mathematical model in both α−β and d−q phase coordinates. The control of flying capacitor voltage is discussed, and the algorithm for generating the reference current is described.

Fig. 1 illustrates the schematic layout of a four-level Shunt Active Power Filter utilizing a Flying Capacitor Multilevel Inverter (SAPF-FCMLI). This system is engineered to suppress harmonic currents and compensate for reactive power arising from nonlinear loads. In the presented study, the nonlinear load takes the form of a three-phase diode rectifier, which is known to generate considerable current harmonics.

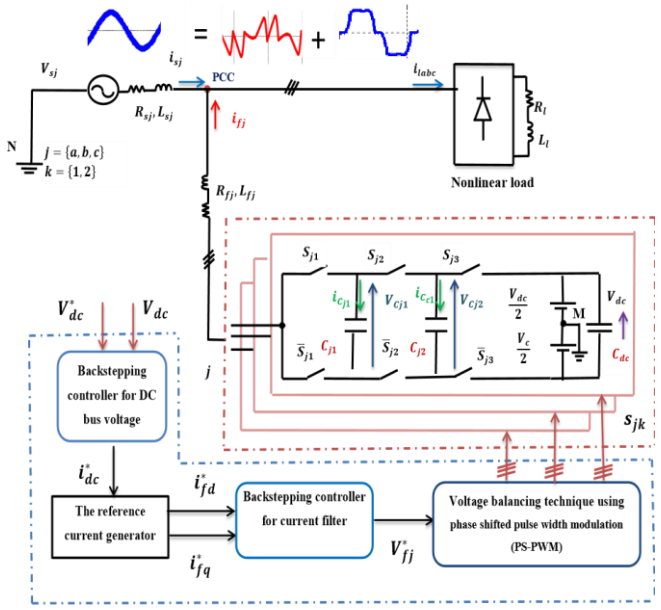

Fig. 1: Three phases SAPF based on Flying Capacitor Multicellular Inverter system.

The SAPF-FCMLI effectively addresses these power quality issues by injecting appropriate compensation currents. As a result, the mains currents remain nearly sinusoidal, even when subjected to nonlinear loading conditions, thereby improving overall power quality and ensuring stable, high-quality source currents.

The FCMLI utilizes two DC-bus capacitors to effectively stabilize the DC bus voltage. The SAPF-FCMLI is connected to the distribution system at a Point of Common Coupling (PCC) through an $(L_{f,j}, R_{f,j})$ coupling filter. The differential equations describing the dynamic model of the three-phase SAPF-FCMLI are defined in $(\alpha\beta)$ axes, as given in Eq. (1).

$$\frac{d}{dt}\begin{pmatrix} i_{f\alpha} \\ i_{f\beta} \end{pmatrix} = \frac{1}{L_f}\begin{pmatrix} v_{s\alpha} - v_{f\alpha} - R_f i_{f\alpha} \\ v_{s\beta} - v_{f\beta} - R_f i_{f\beta} \end{pmatrix} \quad (1)$$

The dynamical model of the system in dq reference frame results in Eq. (2) as follows [18]:

$$\frac{d}{dt}\begin{pmatrix} i_{fd} \\ i_{fq} \end{pmatrix} = \frac{1}{L_f}\begin{pmatrix} v_{fd} - v_{sd} - R_f i_{fd} + \omega L_f i_{fq} \\ v_{fq} - v_{sq} - R_f i_{fq} + \omega L_f i_{fd} \end{pmatrix} \quad (2)$$

According to the Equation (2), the mathematical model of proposed topology three-phase SAPF-FCMLI can be expressed as follows [19]

$$\dot{x} = Ax + Bu + G \quad (3)$$

Equation (3) presents the general state-space form, where x is a state vector (i.e., $[i_{fd}, i_{fq}]^T$), $\dot{x}$ is the reference vector, and u is the input vector (i.e., $[v_{fd}, v_{fq}]^T$). Matrix A, B and G can be expressed as follows:

$$A = \begin{bmatrix} -\frac{R_f}{L_f} & -\omega \\ \omega & -\frac{R_f}{L_f} \end{bmatrix}, B = \begin{bmatrix} \frac{1}{L_f} \\ \frac{1}{L_f} \end{bmatrix}, G = \begin{bmatrix} -\frac{v_{sd}}{L_f} \\ -\frac{v_{sq}}{L_f} \end{bmatrix}$$

G represents external perturbations, such as source voltage variations.

The model presented in (2) describes the interaction between the active filter connected to the PCC and the AC power system in dq coordinates. The mathematical model helps to identify the control inputs, as well as the state and input variables. The model has two inverter currents (i_{fd}, i_{fq}), the control inputs (u_{fd}, u_{fq}) are related to the control signal s_{jk}; and the input voltages at the PCC (v_{sd}, vsq) are treated as external perturbations to the system.

The SAPF injects harmonic currents in opposition to those generated by the nonlinear load. The Synchronous Reference Frame (SRF) method transforms load currents from the $\alpha\beta$ frame to the dq frame to separate harmonic components from the fundamental [11],[20]. This method performs robustly even under non-ideal grid conditions. Fig. 2 presents the block diagram of this extraction method.

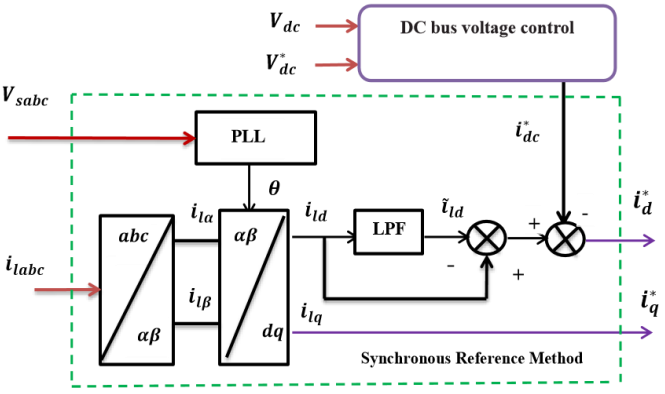

Fig. 2: Block diagram for extracting reference currents under the dq frame.

III. Proposed Backstopping Control

The principle of the backstepping controller involves systematically constructing a control law in an iterative manner. During this process, certain components of the system's state representation are treated as "virtual controls," for which intermediate control laws are progressively developed [21]. This methodology inherently incorporates the concept of Lyapunov stability, ensuring that a chosen Lyapunov function remains positive definite while its time derivative is consistently negative definite. This rigorous approach allows the system to be decomposed into a series of nested subsystems of decreasing order. At each successive step, the order of the system is effectively increased, and the stabilization of the previously unstable parts is addressed, culminating in the derivation of the final control law in the last step. This iterative procedure always guarantees the overall asymptotic stability of the system.

A. Control synthesis by backstepping for DC bus voltage

The DC side of the SAPF-FCMLI can be expressed as:

$$\frac{dV_{dc}}{dt} = \frac{i_{dc}}{c_{dc}} \quad (4)$$

To maintain the DC bus capacitor voltage at a constant desired value, a Backstepping controller is employed for its regulation. The primary objective of this control loop is to generate the power reference at the DC bus capacitor terminal.

The tracking error variable for the DC bus voltage e_{Vdc} is defined as follows:

$$e_{V_{dc}} = V_{dc}^{*} - V_{dc} \tag{5}$$

Its derivative is as follows:

$$\dot{e_{V_{dc}}} = \frac{dV_{dc}^{*}}{dt} + \frac{dV_{dc}}{dt} \tag{6}$$

Substituting $\dot{V_{dc}}$ from (4) into (6) yields:

$$\dot{e_{V_{dc}}} = \dot{V_{dc}} + \frac{i_{dc}}{C_{dc}} \tag{7}$$

To proceed with the Backstepping design, we choose a Lyapunov function V_{L1} as follows:

$$V_{L1} = \frac{1}{2}\, e_{V_{dc}}^{2} \tag{8}$$

The derivative of V_{L1} with respect to time is given by:

$$\dot{V_{L1}} = e_{V_{dc}} \dot{e_{V_{dc}}} = e_{V_{dc}} \left(\dot{V_{dc}^{*}} - \frac{\dot{i_{dc}^{*}}}{C} \right) \tag{9}$$

Lyapunov function must be negative ($\dot{V_{L1}}$<0) this can be achieved by choosing the derivative of the error $eVdc$ to be:

$$\dot{e_{V_{dc}}} = -K_1\, e_{V_{dc}} \tag{10}$$

in which, K_1 is a positive gain (K_1>0).

From equations (7) and (10) we find:

$$\dot{i_{dc}^{*}} = C_{dc} \left(\dot{V_{dc}^{*}} - K_1\, e_{V_{dc}} \right) \tag{11}$$

In this case, the reference voltage V_{dc}^{*} is chosen as a constant, so its derivative $\dot{V_{dc}^{*}}$will be zero. To guarantee the Lyapunov stability, the control law is chosen as:

$$i_{dc}^{*} = C_{dc} K_1\, e_{V_{dc}} \tag{12}$$

Therefore, the control law can be written as given by Eq. (12).

B. Control synthesis by backstepping for current filter

The dynamic equations of the system in the dq reference frame are given by system (2), while the tracking errors for the dq axis currents, e_{id} and e_{iq}, are defined as follows:

$$\begin{cases} e_{i_d} = i_{f_d}^{*} - i_{f_d} \\ e_{i_q} = i_{f_q}^{*} - i_{f_q} \end{cases} \tag{13}$$

Their derivatives are:

$$\begin{cases} \dot{e_{i_d}} = \dot{\imath_{f_d}^{*}} - \dot{\imath_{f_d}} \\ \dot{e_{i_q}} = \dot{\imath_{f_q}^{*}} - \dot{\imath_{f_q}} \end{cases} \tag{14}$$

From system (2), the derivatives of the filter currents $\dot{\imath_{f_d}}$ and $\dot{\imath_{f_q}}$ are as follows:

$$\begin{cases} \dot{\imath_{f_d}} = \frac{1}{L_f} \left(v_{fd} - v_{sd} - R_f i_{fd} + \omega L_f i_{fq} \right) \\ \dot{\imath_{f_q}} = \frac{1}{L_f} \left(v_{fq} - v_{sq} - R_f i_{fq} + \omega L_f i_{fd} \right) \end{cases} \tag{15}$$

The Lyapunov function for this subsystem is chosen as:

$$V_{L2} = \frac{1}{2}\, e_{i_d}^{2} + \frac{1}{2}\, e_{i_q}^{2} \tag{16}$$

The derivative of V_{L2} with respect to time is given by:

$$\dot{V_{L2}} = e_{i_d} \dot{e_{i_d}} + e_{i_q} \dot{e_{i_q}} \tag{17}$$

To ensure the stability of the system, the derivative of the Lyapunov function must be negative $\dot{V}\, L2$ must be negative. This can be achieved by choosing $\dot{e}id$ and $\dot{e}iq$ as:

$$\begin{cases} \dot{e_{i_d}} = K_2 e_{i_d} \\ \dot{e_{i_q}} = K_3 e_{i_q} \end{cases} \tag{18}$$

where, K_2 and K_3 are positive gains (K_2>0, K_3>0).

Substituting $\dot{e_{i_d}}$ and $\dot{e_{i_q}}$ from (14) into (18) and then substituting $\dot{i}fd^{\,*}$ and $\dot{i}fq^{\,*}$ from (15), we derive the expressions for the control inputs vfd and vfq. For example, from the first part of (18) and (14):

$$\dot{\imath_{f_d}} - \frac{1}{L_f} \left(v_{fd} - v_{sd} - R_f i_{fd} + \omega L_f i_{fq} \right) = -K_2 e_{i_d} \tag{19}$$

Rearranging to solve for v_{fd}, it yields:

$$v_{fd} = v_{sd} - R_f i_{fd} + \omega L_f i_{fq} + L_f \left(\dot{\imath_{f_d}} - K_2 e_{i_d} \right) \tag{20}$$

Similarly, for v_{fq}, it follows

$$v_{fq} = v_{sq} - R_f i_{fq} + \omega L_f i_{fd} + L_f \left(\dot{\imath_{f_q}} - K_3 e_{i_q} \right) \tag{21}$$

Therefore, the final control law for the filter voltages v_{fd} and v_{fq} can be written as:

$$\begin{cases} v_{fd} = v_{sd} - R_f i_{fd} + \omega L_f i_{fq} + L_f \left(\dot{\imath_{f_d}^{*}} - i_{f_d} \right) \\ v_{fq} = v_{sq} - R_f i_{fq} + \omega L_f i_{fd} + L_f \left(\dot{\imath_{f_q}^{*}} - i_{f_q} \right) \end{cases} \tag{22}$$

To ensure Lyapunov stability, the control law is given by Equation (19). Flying Capacitor Voltage Balancing using PS-PWM we propose voltage-balancing dynamic in FCMLI using phase shifted pulse width modulation (PS-PWM). We specialize in the case three-cell inverter which represents four-level FCMLI (p=3), the control law balances the flying capacitor voltages to the defined values ($v_{Cj1}^{*} = \frac{V_{dc}}{3}$; $v_{Cj2}^{*} = 2\frac{V_{dc}}{3}$) [11]. The FCMLI employs phase-shifted pulse width modulation for voltage balancing [22, 23]. The voltage balancing dynamics are governed by:

$$\begin{cases} \frac{dV_{Cj1}}{dt} = \frac{1}{C} \left(d_{j2} - d_{j1} \right) i_{f_j} \\ \frac{dV_{Cj2}}{dt} = \frac{1}{C} \left(d_{j3} - d_{j2} \right) i_{f_j} \end{cases} \tag{23}$$

There are two values for the switch control functions. s_{jk}= {0,1}, meaning "1" and "0" that the switch is on and off respectively. The switch pairs in each phase function in a complementary manner s_{j1}, $\overline{s_{j1}}$, s_{j2}, $\overline{s_{j2}}$, and s_{j3}, $\overline{s_{j3}}$,. The line-to-ground voltage V_{Mj} and the currents through the flying capacitors (i_{Cj1}, i_{Cj2}) can be written using Kirchhoff's laws as:

$$V_{Mj} = (s_{j1} - s_{j2})V_{cj1} + (s_{j2} - s_{j3})V_{cj2} + s_{j3}\frac{V_{dc}}{2} - \frac{V_{dc}}{2} \quad (24)$$

From the preceding equations, we deduce that the current flowing through a capacitor is governed by the control signals linked to two consecutive switches within a switching period. The local-average representation of the capacitor current can be expressed as:

$$\begin{cases} \overline{i_{Cj1}} = (d_{j2} - d_{j1})\overline{i_{fj}} \\ \overline{i_{Cj2}} = (d_{j3} - d_{j2})\overline{i_{fj}} \end{cases} \quad (25)$$

Where, $\overline{i_{Cj1}}$ and $\overline{i_{Cj2}}$ are the locally averaged currents of the capacitor d_{j3}, d_{j2} and d_{j1} are the duty cycles of the switch s_{j3}, s_{j2} and s_{j1}, respectively. The duty cycles are modified using proportional control:

$$\begin{cases} d_{j1} = V_{fj}^* + sign(i_{fj})\left(-(V_{cj1}^* - V_{cj1})\right)k_p \\ d_{j2} = V_{fj}^* + sign(i_{fj})\left((V_{cj1}^* - V_{cj1}) - (V_{cj2}^* - V_{cj2})\right)k_p \\ d_{j3} = V_{fj}^* + sign(i_{fj})\left(-(V_{cj2}^* - V_{cj2})\right)k_p \end{cases} \quad (26)$$

Figure 3 shows the diagram of the voltage balancing technique for generation of the functions of the switches s_{jk} [11].

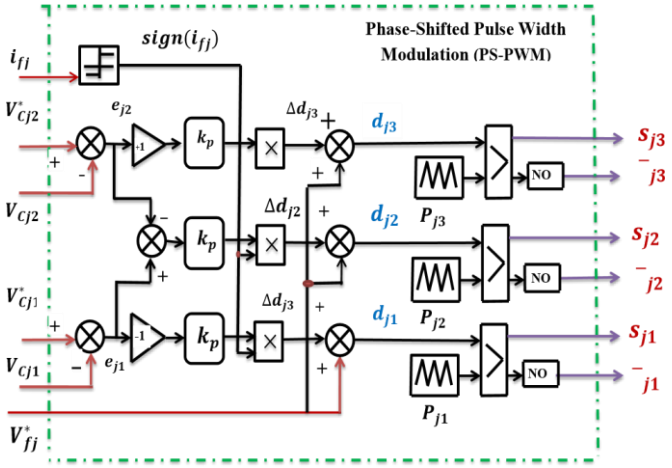

Fig. 3: Block diagram of the voltage balancing technique for four-level multicellular inverter using Phase-Shifted Pulse Width Modulation (PSPWM).

IV. Results and Discussion

The SAPF-FCMLI and its backstepping controller were implemented in MATLAB using the Power Systems Toolbox. The nonlinear load is a three-phase diode rectifier. System parameters are given in Table I.

Table. I
PARAMETERS VALUES OF THE SIMULATED SYSTEM [6]

PARAMETER	VALUE
Supply voltage and frequency	220V, 50 Hz
Supply impedance	1 mΩ, 1 mH
Load impedance	10 Ω, 10 mH
Coupling Filter	1 mΩ, 1 mH
DC bus voltage	800 V
DC bus capacitance	5 mF
Switching frequency	10 kHz
Gains: K1, K2, and K3	10, 70, 70

The objective of this work is to demonstrate the effectiveness of the SAPF-FCMLI controlled by a backstepping controller in terms of harmonic current filtering, reactive power compensation, and source current balancing under unbalanced nonlinear load conditions.

To validate its efficacy and robustness, comprehensive computer simulations were performed, including a significant load change introduced at 0.6 seconds. These simulations assessed the system's dynamic response, harmonic mitigation, and power factor improvement. A key aspect of the evaluation involved a direct comparison between the proposed backstepping controller and a conventional PI controller.

Initially, before SAPF-FCMLI activation (Fig. 4), source currents were heavily distorted with high Total Harmonic Distortion (THD) and were out of phase with the voltage, leading to a low power factor and high reactive power absorption. Upon activation, the SAPF-FCMLI, under both control strategies, dramatically enhanced power quality. Source currents became remarkably sinusoidal and perfectly synchronized with the voltage (Fig. 5 for backstepping, Fig. 6 for PI), indicating significantly reduced reactive power consumption and an excellent power factor.

Quantitatively, the backstepping controller consistently exceeded the PI controller in reducing THD. As detailed in Table II, the backstepping controller achieved a remarkable THD of 0.65% (pre-variation) and 1.02% (post-variation), which was significantly lower than the PI controller's 2.57% (pre-variation) and 2.31% (post-variation). The backstepping controller also maintained RMS currents closer to desired levels across both conditions, affirming its superior harmonic mitigation capabilities and robust control in dynamic scenarios.

Table. II
COMPARISON BETWEEN BACKSTEPPING CONTROLLER BC AND PI CONTROLLER IN TERMS OF SOURCE CURRENT

	PI		BC	
	t< 0.6s	t> 0.6s	t< 0.6s	t> 0.6s
THD (%)	2.57	2.31	0.65	1.02
RMS (A)	54.8	150.4	52.54	147.04

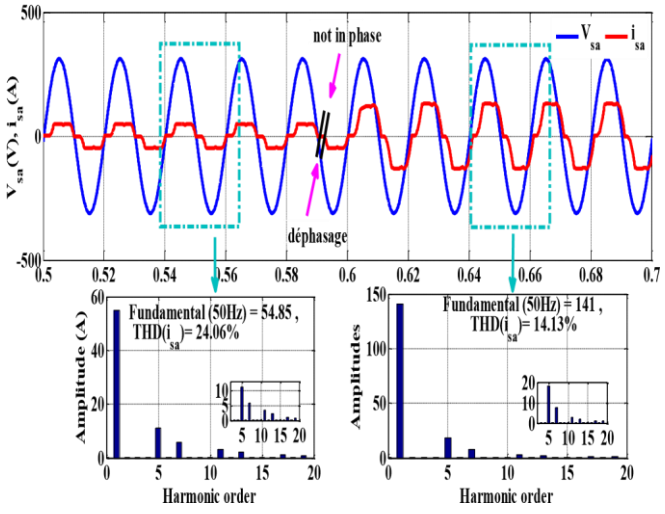

Fig. 4: Voltage and Source current (phase (a)) with THDs before SAPF-FCMLI insertion

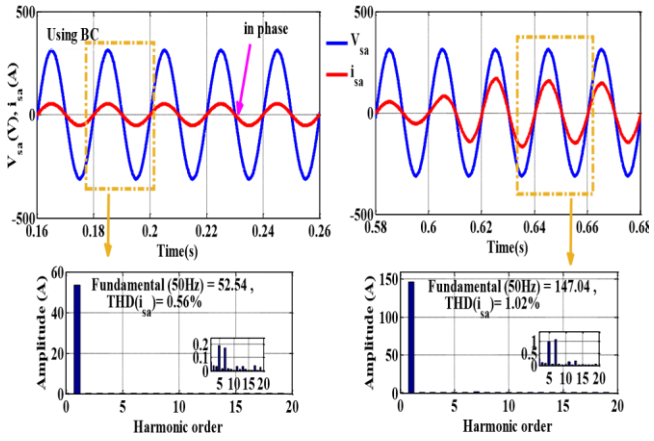

Fig. 5: Source voltage and current (phase (a)) waveforms with corresponding THDs after SAPF-FCMLI insertion using the backstepping controller.

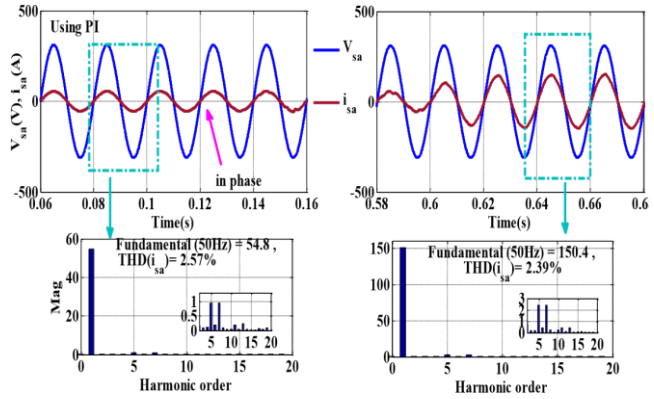

Fig. 6: Voltage and source current (phase (a)) with THDs after SAPFFCMLI insertion using PI controller.

The backstepping controller consistently demonstrates superior voltage regulation performance compared to the PI controller, especially under load disturbances. The DC bus voltage undershoot is a mere 27V with backstepping control, precisely half the 54V observed with PI control. Similarly, flying capacitor voltage (V_{Cj1}, VCj_2) undershoots are consistently half as low with Backstepping, as detailed in Table III.

Table. III

PERFORMANCE COMPARISON BETWEEN BACKSTEPPING CONTROLLER BC AND PI CONTROLLERS IN TERMS OF THE DC BUS VOLTAGE AND FLYING CAPACITOR VOLTAGES

Metric		PI	BC
Transit time		0.32 s	0.18 s
The undershoot in voltage	Vdc	54 V	27 V
	Vcj1	36 V	18 V
	Vcj2	18 V	9 V
Steady-State Error		higher	Significantly lower
Robustness		limited	Superior

Furthermore, the backstepping controller ensures a significantly faster transient response, taking just 0.18 seconds to restore voltages to their reference values, half the 0.32 seconds required by the PI controller. It also minimizes steady-state deviations and voltage ripples in the flying capacitors, crucial for maintaining high output waveform quality and overall system efficiency.

Figs. 7 and 8 visually confirm this stark contrast, with Figure 7 illustrating the backstepping controller's stable and excellent regulation, while Figure 8 highlights the larger fluctuations and slower recovery characteristic of PI control. This evidence collectively underscores the Backstepping controller's enhanced resilience and precision in maintaining critical voltage stability within the SAPF-FCMLI system.

V. CONCLUSION

This paper presented a backstepping control technique for a three-phase SAPF-FCMLI, achieving harmonic mitigation, reactive power compensation, and voltage balancing. Simulation results validate the controller's effectiveness, with THD reduced to 0.65%–1.02%, transient response time of 0.18 s, and near-zero steady-state error. Compared to the PI controller, backstepping offers faster response, lower oscillations, and better stability under nonlinear load variations. The approach enhances power quality, complies with IEEE standards, and improves grid efficiency. Future research could focus on real-time implementation, experimental validation, and integration with other advanced control techniques to further optimize performance.

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